IN THE CLAIMS

What is claimed is:

1. An apparatus comprising:

a decoder configured to decode control signals of a first set of control signal formats, and

a circuit coupled to the decoder, the circuit in response to at least one decoded control signal to convert between a first plurality of numbers in an integer format stored in a first packed register of a first set of architectural registers and a second plurality of numbers in a floating-point format stored in a second packed register of a second set of architectural registers.

2. The apparatus of claim 1, wherein the second plurality of numbers is equal in count to the first plurality of numbers.

3. The apparatus of claim 1, wherein the set of control signal formats permits control signals to convert the second plurality of numbers in a packed floating point format to the first plurality of numbers in a packed doubleword integer data format.

4. The apparatus of claim 3, wherein a difference of numbers between the second plurality and the first plurality are set to zeroes in a packed doubleword integer data format.

5. The apparatus of claim 3, wherein the set of control signal formats permits control signals to identify the first plurality of numbers as two numbers

in the first set of architectural registers each of the first set of architectural registers having 64-bits of storage capacity.

6. The apparatus of claim 3, wherein the set of control signal formats permits control signals to identify the floating point format as a 64-bit double-precision floating point format.

7. The apparatus of claim 1, wherein the set of control signal formats permits control signals to convert the first plurality of numbers in a packed integer format to the second plurality of numbers in a packed floating point data format.

8. The apparatus of claim 7, wherein a difference count of numbers between the second plurality and the first plurality are not converted to a floating point data format.

9. An apparatus comprising:

a first storage area to store packed data, the first storage area representing a register in a first set of architectural registers;

a second storage area to store packed data, the second storage area representing a register in a second set of architectural registers;

a decoder to decode control signals of a first set of control signal formats; and

conversion logic to convert between a first plurality of numbers in an integer format stored in the first storage area and a second plurality of numbers

in a floating-point format stored in the second storage area responsive to the decoding of a control signal of the first set of control signal formats.

10. The apparatus of claim 9, wherein the conversion logic comprises an integrated circuit.

11. The apparatus of claim 9, wherein the conversion logic comprises a combination of an integrated circuit and a sequence of machine executable emulation instructions.

12. The apparatus of claim 11, wherein the first set of control signal formats the decoder is to decode comprise Intel-Architecture control signal formats having three or more bytes, a first byte and a second byte of the three bytes permitting an operation code to specify a conversion operation for converting numbers between a set of packed integer data formats and a set of packed floating point data formats.

13. A processor comprising:

a first register belonging to a first set of architectural registers;

a second register belonging to a second set of architectural registers;

a decoder to decode instructions; and

a floating point arithmetic circuit coupled to the decoder, the floating point arithmetic circuit in response to at least one first decoded instruction configurable to,

access a first plurality of numbers in a packed floating point format in the first register;

convert the first plurality of numbers to a second plurality of numbers in an integer format; and

store the second plurality of numbers in a packed integer format in the second register.

14. The processor of claim 13, wherein the floating point arithmetic circuit in response to at least one second decoded instruction being configurable to,

access a first one of the first plurality of numbers in the packed floating point format in the first register;

convert the first one of the first plurality of numbers to a second number in an integer format; and

store the second number in a packed integer format in the second register.

15. The processor of claim 13, wherein the floating point arithmetic circuit in response to at least one second decoded instruction being configurable to,

access a third plurality of numbers in a packed integer format in the second register;

convert the third plurality of numbers to a fourth plurality of numbers in a floating point format; and

store the fourth plurality of numbers in a packed floating point format in the first register.

16. The processor of claim 15, wherein the floating point arithmetic circuit in response to at least one third decoded instruction being configurable to,

access a first one of the third plurality of numbers in the packed integer format in the second register;

convert the first one of the third plurality of numbers to a second number in a floating point format; and

store the second number in a packed floating point format in the first register.

17. A computer system comprising:

a memory to store a packed conversion instruction of a first set of control signal formats permitting a first source address and a second destination address, the packed conversion instruction being of a set of packed conversion instructions to convert between a set of packed floating point data formats and a set of packed integer data formats;

a storage device to store a software installation, the software installation configured to supply the packed conversion instruction to the memory for execution;

a processor to receive and decode the packed conversion instruction from the memory, the processor including:

a first storage location corresponding to the first source address to store a first packed data having a first plurality of packed data elements including a first data element of a first data format,

a second storage location corresponding to the second destination address to store a second packed data having a second plurality of packed data elements including a second data element of second data format, and

conversion logic to receive the first packed data from the first storage

location and to convert the first data element to the second data element and to store the second data element in the second storage location.

18. The computer system of claim 17, wherein the conversion logic comprises an integrated circuit.

19. The computer system of claim 17, wherein the first set of control signal formats comprise Intel-Architecture control signal formats having three or more bytes, a first byte and a second byte of the three bytes permitting an operation code to specify a conversion operation for converting numbers between a set of packed integer data formats and a set of packed floating point data formats.

20. The computer system of claim 19, wherein the conversion logic comprises a combination of an integrated circuit and a sequence of machine executable emulation instructions.

21. The computer system of claim 19, wherein the set of packed conversion instructions includes an instruction (CVTPD2PI) to convert data of a packed double-precision floating-point data format to data of a packed doubleword integer data format.

22. The computer system of claim 19, wherein the set of packed conversion instructions includes an instruction (CVTPI2PD) to convert data of a packed doubleword integer data format to data of a packed double-precision floating-point data format.

23. The computer system of claim 19, wherein the set of packed conversion instructions includes an instruction (CVTTPD2PI) to convert data of a packed double-precision floating-point data format to data of a packed doubleword integer data format using truncation when a result element exceeds the maximum signed doubleword integer value.

24. The computer system of claim 19, wherein the set of packed conversion instructions includes an instruction (CVTPD2DQ) to convert data of a packed double-precision floating-point data format to data of a packed doubleword integer data format.

25. The computer system of claim 19, wherein the set of packed conversion instructions includes an instruction (CVTDQ2PD) to convert data of a packed doubleword integer data format to data of a packed double-precision floating-point data format.

26. The computer system of claim 19, wherein the set of packed conversion instructions includes an instruction (CVTTPD2DQ) to convert data of a packed double-precision floating-point data format to data of a packed doubleword integer data format using truncation when a result element exceeds the maximum signed doubleword integer value.

27. The computer system of Claim 18, wherein the conversion logic comprises;

a right shifter to receive a number in a floating point format and to

accommodate a shift beyond a data path width required by a floating point arithmetic operation.

28. The computer system of Claim 27, wherein the floating point format is a double precision format.

29. The computer system of Claim 18, the conversion logic further comprising a left shifter to receives a number in the integer format, to accommodate a shift beyond the data path width required by a floating point arithmetic operation.

30. The computer system of Claim 29, wherein the integer format is a 64-bit signed integer format.